METHOD OF FABRICATING DUAL DAMASCENE INTERCONNECTIONS OF MICROELECTRONIC DEVICE USING HYBRID LOW K-DIELECTRIC AND CARBON-FREE INORGANIC FILLER

This application is a continuation-in-part (CIP) of Application serial Nos. 10/081,661 filed on February 22, 2002, 10/114,274 filed on April 2, 2002 and 10/437,529, filed on May 14, 2003, assigned to the assignee of the present application, the contents of which are incorporated herein by reference in their entirety.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a microelectronic device, and more particularly, to a method of fabricating dual damascene interconnections of a microelectronic device.

2. Description of the Related Art

As microelectronic devices become more efficient and highly integrated, multi-layered interconnections are more widely used. To obtain a reliable device including multi-layered interconnections, each interconnection layer are formed in a planar fashion. Thus, dual damascene interconnections have become strongly relied upon.

Meanwhile, in today's highly integrated microelectronic devices, a design rule has been reduced to 0.18 μm or less, and even to 90 nm. Such a small design rule brings about increases in RC delay, cross talk, and power consumption. To solve these problems, an interlayer dielectric (ILD) should be formed of a low-k dielectric material layer. As a result, the need to further develop techniques of fabricating dual damascene interconnections using a low-k ILD has greatly increased.

Methods of fabricating dual damascene interconnections are disclosed in U.S. Patent No. 6,057,239, and in J. Vac. Sci. Technol. A19 (2001) p. 1388, by P. Jiang et al. However, the method disclosed in U.S. Patent No. 6,057,239 uses an ILD formed of only an oxide layer, a dielectric constant of which is about 4 to 4.3.

Also, when a trench is etched and cleaned, an etch stop layer may be etched to expose interconnections, thus degrading electrical properties of the interconnections. In the thesis by P. Jiang et al., before a trench is etched, a via is filled with an organic filler, such as a bottom anti-reflection layer (ARL), to prevent degradation of electrical properties. However, because both the organic filler and a photoresist pattern are organic materials having similar etch rates, the photoresist pattern is almost removed during etching of the organic filler formed on an ILD. Thus, when the ILD is etched to form a final trench, the photoresist pattern cannot be used as an etch mask. To prevent this problem, as shown in FIG. 1A, before a photoresist pattern 22 is formed, an organic filler 20 is etched using an etchback process until the organic filler 20 remains only in a via 19. However, this process is very complicated. In addition, as illustrated with dotted circles 24 in FIG. 1B, a low-k ILD 18 is not etched and remains on the organic filler 20 because of a difference in etch rate between the organic filler 20 and the low-k ILD 18. The remaining low-k ILD 18 generates fences 26 as shown in FIG. 1C. In FIGS. 1A and 1B, reference numeral 10 denotes a substrate, 12 denotes a lower ILD, 14 denotes lower interconnections, and 16 denotes an etch stop layer.

To prevent the fence defects, if the organic filler 20 is etched back by over-etching such that a portion of the via 19 is filled with the organic filler 20, a thickness deviation of a photoresist layer becomes very great between a high via-density region and a low via-density region. As a result, a depth of focus (DOF) margin decreases in a photolithographic process.

Further, during an exposure process for forming the photoresist pattern 22, basic materials, such as amine, may be diffused from the ILD 18 through the organic filler 20 to the photoresist layer, thereby resulting in photoresist poisoning.

Therefore, a method of fabricating reliable dual damascene interconnections without degrading electrical properties of a low-k ILD is required.

SUMMARY OF THE INVENTION

The present invention provides a method of fabricating reliable dual damascene interconnections in a low-k interlayer dielectric (ILD).

The present invention also provides a method of fabricating non-defective dual damascene interconnections.

In accordance with an aspect of the present invention, there is provided a method of fabricating dual damascene interconnections, which comprises (a) forming a hybrid dielectric layer having a dielectric constant of 3.3 or less on a substrate; (b) forming a via in the dielectric layer; (c) filling the via with a carbon-free inorganic filler; (d) partially etching the inorganic filler filling the via and the dielectric layer to form a trench, which is connected to the via and in which interconnections will be formed; (e) removing the inorganic filler remaining in the via; and (f) completing interconnections by filling the trench and the via with an interconnection material.

In accordance with another aspect of the present invention, there is provided a method of fabricating dual damascene interconnections, which comprises (a) forming an organo silicate glass layer on a substrate; (b) forming a via in the organo silicate glass layer; (c) filling the via with an HSQ-based filler; (d) partially etching the HSQ-based filler filling the via and the organo silicate glass layer to form a trench, which is connected to the via and in which interconnections will be formed; (e) removing the HSQ-based filler remaining in the via; and (f) completing interconnections by filling the trench and the via with an interconnection material.

Preferably, the organo silicate glass layer is formed using chemical vapor deposition (CVD).

In accordance with yet another aspect of the present invention, there is provided a method of fabricating dual damascene interconnections, which comprises (a) forming a lower interconnection on a substrate; (b) forming an etch stop layer on the lower interconnection; (c) forming an organo silicate glass layer using chemical vapor deposition (CVD) on the etch stop layer; (d) forming a via through the organo silicate glass layer to expose the etch stop layer; (e) filling the via with an HSQ-based filler; (f) processing the surface of the HSQ-based filler using plasma; (g) forming an anti-reflection layer (ARL) on the plasma-processed surface of the HSQ-based filler; (h) partially etching the ARL, the HSQ-based filler filling the via, and the organo silicate glass layer to form a trench, which is connected to the via and in which interconnections will be formed; (i) removing the HSQ-based filler remaining in the via; and (k)

completing interconnections by filling the trench and the vias with an interconnection material.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other objects, features and advantages of the invention will be apparent from the more particular description of a preferred embodiment of the invention, as illustrated in the accompanying drawings in which like reference characters refer to the same parts throughout the different views. The drawings are not necessarily to scale, emphasis instead being placed upon illustrating the principles of the invention.

FIGS. 1A through 1C are cross-sectional views and a scanning electron microscope (SEM) image illustrating a conventional method of fabricating conventional dual damascene interconnections.

FIGS. 2 through 13 are cross-sectional views illustrating a method of fabricating dual damascene interconnections according to an embodiment of the present invention.

FIGS. 14A, 14B, 15A, 16A, 17A, 17B, 18 and19 are SEM images showing a test sample fabricated according to the present invention.

FIGS. 15B and 16B are SEM images showing a contrastive sample according to a conventional method.

FIGS. 20 through 24 are graphs showing electrical properties of a device fabricated according the present invention.

DETAILED DESCRIPTION OF THE INVENTION

In the present invention, an interlayer dielectric (ILD) may be formed of a hybrid low-k dielectric material. The hybrid low-k dielectric material has advantages of both organic and inorganic materials. The hybrid low-k dielectric material shows low-k characteristics like an organic material. Also, the hybrid low-k dielectric material can be formed using a conventional apparatus and process since it has a modified structure from a conventional inorganic silicate oxide. And, the hybrid low-k dielectric material is thermally stable like an inorganic material. In particular, when the ILD is formed of a

hybrid low-k dielectric material, whose dielectric constant is 3.3 or lower, RC delay is prevented and cross talk and power consumption can be minimized.

In the embodiments of the present invention, a via filler may be formed of a material which has a good gap filling characteristic and which has an etch rate substantially equal to that of a low-k ILD, or has a high etch selectivity with respect to the low-k ILD, depending on etching methods or conditions. In particular, the via filler may be formed of a carbon-free inorganic material so that it can be dry etched at the same etch rate as the ILD and wet etched at a much higher rate than the ILD. Also, the via filler may be formed of a material that can function as a barrier layer to basic materials, such as nitrogen and amine. In specific embodiments of the present invention, a via filler may be formed of a material comprising a light absorption material or a dissolution inhibitor for a photoresist developing solution. Thus, an etch stop layer for protecting a lower interconnection is not damaged, photoresist poisoning is prevented, a DOF margin is improved in a photolithographic process, and fence defects, which adversely affect electrical properties of dual damascene interconnections, are prevented. Further, robust and reliable dual damascene interconnections can be fabricated, without increasing the critical dimension of a trench.

The present invention can be applied to microelectronic devices, such as highly integrated circuit semiconductor devices, processors, micro electromechanical (MEM) devices, optoelectronic devices, and display devices. In particular, the present invention is highly useful for devices requiring high-speed characteristics, such as central processing units (CPUs), digital signal processors (DSPs), combinations of a CPU and a DSP, application specific integrated circuits (ASICs), logic devices, and SRAMs.

Herein, an opening exposing a lower interconnection is referred to as a via, and a region where interconnections will be formed is referred to as a trench. Hereinafter, the present invention will be described by way of an example of a via-first dual damascene process, in which, even if misalignment occurs, the size of a via can be held constant.

Hereinafter, a method of fabricating dual damascene interconnections according to an embodiment of the present invention will be described with reference to FIGS. 2 through 13.

As shown in FIG. 2, a substrate 100 is prepared. A lower ILD 105 including a lower interconnection 110 is formed on the substrate 100. The substrate 100 may be, for example, a silicon substrate, a silicon on insulator (SOI) substrate, a gallium arsenic substrate, a silicon germanium substrate, a ceramic substrate, a quartz substrate, or a glass substrate for display. Various active devices and passive devices may be formed on the substrate 100. The lower interconnection 110 may be formed of various interconnection materials, such as copper, copper alloy, aluminium, and aluminium alloy. The lower interconnection 110 is preferably formed of copper because of its low resistance. Also, the surface of the lower interconnection 110 is preferably planarized.

Referring to FIG. 3, an etch stop layer 120, a low-k ILD 130, and a capping layer 140 are sequentially stacked on the surface of the substrate 100 where the lower interconnection 110 is formed, and a photoresist pattern 145 is formed on the capping layer 140 to define a via.

The etch stop layer 120 is formed to prevent electrical properties of the lower interconnection 110 from being damaged during a subsequent dry etch process for forming a via and a subsequent wet etch process for removing the remaining filler. Accordingly, the etch stop layer 120 is formed of a material having a high etch selectivity with respect to the ILD 130 formed thereon. Preferably, the etch stop layer 120 is formed of SiC, SiN, or SiCN, having a dielectric constant of 4 to 5. The etch stop layer 120 is as thin as possible in consideration of the dielectric constant of the entire ILD, but thick enough to properly function as an etch stop layer.

The ILD 130 is formed of a hybrid low-k dielectric material, which has advantages of organic and inorganic materials. That is, the ILD 130 formed of the hybrid low-k dielectric material has low-k characteristics, can be formed using a conventional apparatus and process, and is thermally stable. The ILD 130 is formed of a hybrid material having a dielectric constant of 3.3 or less, to prevent an RC delay between the lower interconnection 110 and dual damascene interconnections and minimize cross talk and power consumption. Most preferably, the ILD 130 is formed of low-k organo

silicate glass (OSG). The ILD 130 formed of low-k OSG can be formed using chemical vapor deposition (CVD), more specifically, plasma-enhanced CVD (PECVD). As the carbon content in an OSG layer increases, the dielectric constant of the OSG layer decreases but thermal and mechanical characteristics are degraded. However, if an OSG layer is formed using CVD, the carbon content in the OSG layer can be adjusted to appropriately control the dielectric constant and thermal and mechanical characteristics of the OSG layer. Therefore, an OSG layer formed using CVD is suitable for the ILD 130. It is obvious that various changes may be made by known methods in the source gas (e.g., carbon source gas, silicon source gas, and oxygen source gas), a CVD chamber, and fabricating conditions (e.g., temperature and time conditions) used for forming the OSG layer using CVD. A method of forming OSG using CVD may be a known method or methods disclosed in U.S. Patent No. 6,455,445, No. 6,432,846, No. 6,514,880, No. 6,559,520, No. 6,352,945, No. 6,383,955, and No. 6,410,463, and Korean Patent No. 0364053, which are incorporated herein by reference in their entirety as fully disclosed in the present invention. The ILD 130 is formed to a thickness of 3000 Å to 20000 Å, preferably, 6000 Å to 7000 Å. However, the ILD 130 can be formed to various thicknesses by those skilled in the art.

Meanwhile, when dual damascene interconnections are planarized using chemical mechanical polishing (CMP), the capping layer 140 prevents the ILD 130 from being damaged by the CMP. Thus, the capping layer 140 is formed of SiO_2, SiOF, SiON, SiC, SiN, or SiCN. Preferably, the capping layer 140 functions as an anti-reflection layer (ARL) in a subsequent photolithographic process for forming a trench. Accordingly, the capping layer 140 is more preferably formed of SiO_2, SiON, SiC, or SiCN. However, if damage to the ILD 130 can be prevented by controlling the CMP process and an anti-reflective material layer is formed in a subsequent process, the formation of the capping layer 140 may be optionally omitted.

The photoresist pattern 145 is formed by forming a layer of a photoresist that is suitable for a light source of 248 nm or less and then performing exposure and developing processes using a photo mask defining a via.

Referring to FIG. 4, the ILD 130 is dry etched (147) using the photoresist pattern 145 as an etch mask to form a via 150. The ILD 130 is etched using a reactive ion

beam etch (RIE) process, which uses a mixture of a main etch gas (e.g., CxFy and CxHyFz), an inert gas (e.g. Ar gas), and optionally at least one of O_2, N_2, and COx. Here, the RIE conditions are adjusted such that only the ILD 130 is selectively etched and the etch stop layer 120 is not etched.

Referring to FIG. 5, the photoresist pattern 145 is removed and the via 150 is filled with a via filler 160. The photoresist pattern 145 is processed using an H_2-based plasma and removed using a stripper. H_2-based plasma refers to plasma obtained from H_2, N_2/H_2, NH_3/H_2, NH_3/H_2, He/H_2, or a mixture thereof. If the photoresist pattern 145 is removed using O_2-ashing, which is widely used for removing a photoresist pattern, the ILD 130 containing carbon to have organic properties may be damaged by the O_2-based plasma. Thus, the photoresist pattern 145 is preferably removed using an H_2-based plasma.

The via filler 160 is formed of a material that has a good gap filling characteristic. Also, a dry etch ratio of the via filler 160 to the ILD 130 is either about 1:1 or 4:1 or less. Further, the via filler 160 is formed of a material that is etched at a higher etch rate than the ILD 130 in a subsequent wet etch process. Preferably, the via filler 160 is formed of a material having such a characteristic that a wet etch ratio of the via filler 160 to the ILD 130 is 20:1 or higher. Also, during an exposure process for forming a photoresist pattern to define a subsequent trench, basic materials, such as nitrogen and amine, included in the ILD 130, may diffuse into a photoresist layer. Thus, the via filler 160 is formed of a material that can prevent the diffusion of the basic material into the photoresist layer. That is, the via filler 160 is preferably formed of a carbon-free inorganic material to have a dry etch rate being substantially equal to that of the ILD 130, which is a hybrid of an organic material and an inorganic material, and a wet etch rate being much higher than that of the ILD 130. Given the foregoing conditions, HydrogenSilsesQuioxane (HSQ) is the most suitable for the via filler 160 among carbon-free inorganic materials.

Further, the via filler 160 preferably includes a light absorption material or a dissolution inhibitor. The dissolution inhibitor, which inhibits dissolution of a photoresist developing solution, may be a material known by those skilled in the art. The functions of the light absorption material and the dissolution inhibitor will be described later. In

the present invention, HSQ-based materials refer to not only pure HSQ but also HSQ including additives, such as a light absorption material and/or a dissolution inhibitor.

The via filler 160 is formed using spin coating to completely fill the via 150. While it is possible to fill only the via 150 with the via filler 160, the via filler 160 is preferably formed on the capping layer 140 to a predetermined thickness in consideration of process margin control. Also, it is preferable in terms of a DOF margin that a difference between the height T1 of the via filler 160 formed in a low via-density region and the height T2 of the via filler 160 formed in a high via-density region is 2000 Å or less. The thickness of HSQ-based materials can be easily controlled in consideration of variables such as coating recipe, the space between vias 150, the critical dimension, and the height of the via 150, and the condition ($T1-T2 \leq 2000$ Å) can be easily satisfied.

Referring to FIG. 6, the surface of the via filler 160 is processed using plasma 170. The plasma 170 is derived from O_2, H_2, He, NH_3, N_2, Ar, or any mixture thereof, and the plasma processing is conducted at a temperature of room temperature to 500 °C for 1 to 120 seconds. The surface of the via filler 160 is densified by the plasma processing. Also, the plasma processing is carried out to prevent a photoresist developing solution from dissolving the via filler 160. Accordingly, if the via filler 160 includes a dissolution inhibitor, the plasma processing may be optionally omitted.

Referring to FIG. 7, an anti-reflection layer (ARL) 180 is formed on the via filler 160, which is processed using plasma 170. Although it is possible to form the ARL 180 using an inorganic material, the ARL 180 is preferably formed of an organic material in order to be easily removed later. The ARL 180 is formed of an anti-reflective material that can absorb light of a wavelength 248 nm, 193 nm, or less, which is known to those skilled in the art, or a material that is disclosed in U.S. Patent Application No. 10/400,029, commonly owned by the same assignee and is incorporated herein by reference in its entirety as fully disclosed in the present invention. The ARL 180 is formed to a thickness of 500 Å to 700 Å.

Referring to FIG. 8, a photoresist layer 185 is formed and then exposed to light using a mask 200 defining a trench. When the light emitted from an exposure source

with a wavelength of 248 nm, 193 nm, or less is transmitted through a transmission region 201 of the mask 200 and radiated onto the photoresist layer 185, acids H+ are generated from a photo acid generator included in an exposure portion 185b of the photoresist layer 185. Here, the ARL 180, disposed under the exposure portion 185b, prevents rays penetrating the photoresist layer 185 from being reflected back to the photoresist layer 185. Accordingly, if the via filler 160 includes a light absorption material to prevent the reflection of rays, the formation of the ARL 180 may be optionally omitted. The acids H+ generated in the exposure portion 185b hydrolyze the photoresist layer 185 into a material soluble in a developing solution. After the exposure process, acidolysis becomes more active by a post-exposure baking (PEB) process. During the exposure process and the PEB process, the via filler 160 functions as a diffusion barrier layer to nitrogen or amine. Accordingly, basic materials, such as nitrogen and amine, which remain in the ILD 130 due to etch gas used for etching the via 150 as well as the plasma processing for removing the photoresist pattern (145 of FIG. 4) defining the via 150, cannot diffuse as depicted in a dotted line through the via filler 160 and neutralize the acids H+ generated in the exposure portion 185b, since the via filler 160 functions as the diffusion barrier layer, thereby resulting in no photoresist poisoning.

Referring to FIG. 9, a photoresist pattern 185a is formed. When the post-exposure baked photoresist layer 185 is soaked in a tetramethyl ammonium hydroxide developing solution, only the exposure portion 185b is dissolved in the developing solution. Thus, as shown in FIG. 9, the photoresist pattern 185a is obtained. Here, the via filler 160 is not exposed to the developing solution due to the ARL 180 disposed under the exposure portion 185b. If the via filler 160 is processed using plasma or includes a dissolution inhibitor, it is not damaged by the developing solution even without the ARL 180.

FIG. 10 shows the formation of a trench 190. The ARL 180, the via filler 160, and the capping layer 140 are sequentially etched using the photoresist pattern 185 as an etch mask, and then the ILD 130 and the via filler 160 are etched to a predetermined depth, thereby forming the trench 190. The trench 190 is dry etched on condition that an etch ratio of the ILD 130 to the via filler 160 is 1:1, or 4:1 or less. Therefore, fence

defects (see FIG. 1) can be prevented and, since a portion of the via filler 160 still remains in the via 150, it can prevent the etch stop layer 120 from being etched to damage the lower interconnection 110. If the ILD 130 is formed of an OSG and the via filler 160 is formed of an HSQ-based material, both of them have characteristics of inorganic materials. Thus, if an RIE process is carried out using a mixture of a main etch gas (e.g., CxFy and CxHyFz), an inert gas (e.g. Ar gas), and optionally at least one of O_2, N_2, and COx, the foregoing condition for etching the trench 190 can be satisfied.

FIG. 11 is a cross-sectional view of the resultant structure, from which the photoresist pattern 185a and the remaining via filler 160 are removed. After the etching of the trench 190 is completed, the photoresist pattern 185a is removed using H_2-based plasma obtained from H_2, N_2/H_2, NH_3/H_2, NH_3/H_2, He/H_2, or a mixture thereof. Next, the via filler 160 is removed, thereby forming a dual damascene interconnection region 195, which includes the via 150 and the trench 190. The via filler 160 is removed using a wet etch process. The wet etch process for removing the via filler 160 is carried out on condition that the ILD 130 is only slightly etched and only the via filler 160 is selectively removed, i.e., that a wet etch ratio of the via filler 160 to the ILD 130 is 20:1 or higher. Also, the via filler 160 should have an etch selectivity with respect to the etch stop layer 120. While the ILD 130 has organic characteristics, the via filler 160 and the etch stop layer 120 are formed of inorganic materials. Thus, to satisfy the condition, the via filler 120 is removed by wet etching using an etchant having a high selectivity with respect to organic materials. In particular, if the via filler 160 is formed of an HSQ-based material, the ILD 130 is formed of an OSG, and the etch stop layer 160 is formed of SiC(N), the via filler 160 may be wet etched in an HF solution diluted with deionized water (DIW), or a buffered oxide etchant (BOE), which is a mixture of NH_4, HF, and deionized water. Preferably, the diluted HF solution is in a ratio of 100 (DIW):1(HF) or higher. Thus, an etch ratio of HSQ-based material to OSG to SiC(N) can be higher than 100:1:1. In addition, etching of the ILD 130 can be prevented during the removal of the via filler 160 so as to precisely control the critical dimension of the trench 190.

A detailed description of the via etching, the trench etching, and the wet etching is given in Korean Patent Application No. 2002-57192, commonly owned by the same

assignee and incorporated herein by reference in its entirety as fully disclosed in the present invention.

Referring to FIG. 12, the etch stop layer 120 exposed in the via 150 is etched until the lower interconnection 110 is exposed, thereby completing the dual damascene interconnection region 195. The etch stop layer 120 is etched so that the lower interconnection 110 is not affected and only the etch stop layer 120 is selectively removed.

Referring to FIG. 13, a conductive layer is formed on the dual damascene interconnection region 195 and then planarized, thereby forming a dual damascene interconnection 210. The conductive layer is formed of aluminum, tungsten, copper, or any alloy thereof, and most preferably formed of copper because of its low resistance. Also, the conductive layer may be a stack of a diffusion barrier layer and a main interconnection layer, or may be embodied in various other forms by known methods.

It is obvious that the via-first dual damascene process described with reference to FIGS. 2 through 13 can be applied to a trench-first dual damascene process.

The present invention will be described in more detail with reference to the following experimental examples. Here, it is obvious that the present invention is not limited to the experimental examples.

The following experimental examples were obtained in a process of fabricating dual damascene interconnections of a 90 nm-design-rule logic device with embedded $1.1\mu m^2$ 6Tr-SRAM.

Experimental example 1

An etch stop layer was formed using SiC(k=5.0), an ILD was formed of CVD OSG(k=2.9) to a thickness of 7000 Å, and a via having a diameter of 0.132 μm was formed. Next, HSQ(Fox™ of Dow Corning Corp.) for a via filler was formed using spin coating. FIGS. 14A and 14B are SEM images showing cross-sectional views of a test sample, in which the HSQ via filler is filled. Referring to FIGS. 14A and 14B, it can be seen that the HSQ had a good gap filling characteristic and was formed in a planar

fashion on an OSG layer. Also, a difference between the thickness T1 (FIG. 14A) of the HSQ layer formed in the low via-density region and the thickness T2 (FIG. 14B) of the HSQ layer formed in the high via-density region was 2000 Å or less.

Experimental example 2

An HSQ layer was formed in the same manner as in Experimental example 1, and then an organic ARL and a photoresist for KrF were sequentially formed on the HSQ layer. An exposure process was conducted using an exposure source with a wavelength of 248 nm and a development process was carried out using a tetramethyl ammonium hydroxide developing solution, thereby forming a photoresist pattern defining a trench. As a result, a test sample was prepared.

A contrastive sample was prepared by forming a photoresist pattern defining a trench directly on an HSQ layer.

FIG. 15A is an SEM image of the test sample, while 15B is an SEM image of the contrastive sample. FIGS. 15A and 15B confirm that a reliable photoresist pattern was obtained by forming an organic ARL.

Experimental example 3

An HSQ layer was formed in the same manner as in Experimental example 1, the surface of the HSQ layer was processed using plasma, and an organic ARL was formed. Next, a photoresist for KrF was coated on the organic ARL. An exposure process was conducted using an exposure source with a wavelength of 248 nm and a development process was carried out using a tetramethyl ammonium hydroxide developing solution, thereby forming a photoresist pattern defining a trench. As a result, a test sample was prepared.

A contrastive sample was prepared by using an organic ARL for a via filler in place of an HSQ layer and forming a photoresist pattern.

FIG. 16A is an SEM image of the test sample, while 16B is an SEM image of the contrastive sample. Referring to FIG. 16A, the HSQ via filler functioned as a diffusion barrier layer to basic materials, such as amine, so that a reliable photoresist pattern could be formed. In contrast, referring to FIG. 16B, when the organic ARL was used

as the via filler, basic materials diffused and neutralized acids H+ in a photoresist layer, thereby forming a damaged photoresist pattern.

Experimental example 4

A photoresist pattern was formed in the same manner as in Experimental example 3, and a trench was formed by performing a dry etch process using a CxFy main etch gas such that an etch ratio of HSQ:OSG was 1:1. Thus, a test sample was prepared. FIGS. 17A and 17B are SEM images of the test sample. FIG. 17A is a cross-sectional view taken along the width of the trench, while FIG. 17B is a cross-sectional view taken along the length of the trench. Referring to FIGS. 17A and 17B, it can be seen that a good trench profile was formed in a dual damascene region, and although over-etching of about 50 % occurred, the HSQ via filler reliably protected a SiC etch stop layer.

Experimental example 5

A trench was formed in the same manner as in Experimental example 4, an HSQ layer remaining in a via was removed using a diluted HF solution in a ratio of 500(DIW):1(HF). Thus, a test sample was prepared. FIG. 18 is an SEM image of the test sample. Referring to FIG. 18, the HSQ layer was completely removed, and a robust and reliable dual damascene region having a good profile and a desired critical dimension was formed without generation of fences.

Experimental example 6

A dual damascene region was formed according to a process of fabricating a test sample as in Experimental examples 1 - 5, and a copper interconnection was formed in the dual damascene region, using a typical copper interconnection fabrication process. The dual damascene interconnection fabrication process was repeated two or more times, thereby completing 9-level dual damascene interconnections of a 90 nm-design-rule logic device with embedded 1.1μm^2 6Tr-SRAM. FIG. 19 is an SEM

image of the logic device. FIG. 19 confirms that non-defective and reliable devices with a fine design rule can be fabricated according to the method of the present invention.

Experimental example 7

Electrical characteristics of the device fabricated in Experimental example 6 were measured. FIGS. 20 through 24 show the results.

Referring to FIGS. 20 and 21, it can be seen that the resulting dual damascene structure had good via resistance characteristics.

Referring to FIG. 22, it can be seen that even if the resulting device was annealed at a temperature of 400°C for 6 hours, the via resistance characteristics were not degraded.

In another method, a device was formed in the same manner as in Experimental example 6, except that the line and the space of interconnections were changed to 0.14 μm and 0.12μm, respectively. FIG. 23 shows results of measuring sheet resistance and leakage current of the interconnections.

Referring to FIG. 23, the sheet resistance and the leakage current were in good condition.

FIG. 24 shows an RC value of the device fabricated according to Experimental example 6 and an RC value of a device in which an etch stop layer is formed of SiN and an ILD is formed of SiOF.

Referring to FIG. 24, when the etch stop layer was formed of SiC and the ILD was formed of OSG as in the present invention, an RC value was reduced to about 20 % compared with the conventional device in which the etch stop layer is formed of SiN and the ILD is formed of SiOF.

According to the present invention, an ILD is formed of a low-k dielectric material such that an RC delay is prevented and cross talk and power consumption can be minimized. Also, the ILD is formed of a hybrid low-k dielectric material and a via filler is formed of a carbon-free inorganic material. As a result, an etch stop layer covering a lower interconnection is protected, photoresist poisoning is prevented, a DOF margin is

improved in a photolithographic process, fences, which may adversely affect electrical properties of dual damascene interconnections, are prevented, and the width and the critical dimension of a trench can be held constant.

While the present invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those of ordinary skill in the art that various changes in form and details may be made therein without departing from the spirit and scope of the present invention as defined by the following claims.